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Designing and simulation of low and rapid voltage comparator

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Abstract: *Dynamic comparators are used widely in lots of circuits and systems. They have a high speed performance with positive feedback structure. Analog to digital convertors, regulator switches, memories and processors can be mentioned as their applications.Important parameters that are considerable in dynamic comparators are offset voltage, lag time and the speed of comparator.In this article the offset voltage, the compare speed and the lag time of two popular comparator, Strong Arm and Double Thiel, have been surveyed. Finally a rapid and low voltage comparator has been designed. For designed comparator in Vcm=1(mV) and VDD=1.2 (V) circumstances the lag time and offset voltage have been obtained equal to 162(ps) and 3.65 (mV) respectively. The parameters of dynamic comparators were simulated and surveyed by the Cadence Virtuoso XL and Hspice software in nmCMOS 180 technology.*

Keywords: *offset voltage, kickback noise voltage, lag time, velocity*

I. Introduction

Nowadays,along with the electronic science advancement, some circuits are needed to make relationship between the analog and digital world in digital domain. Achieving this aim, therefore, the more comparators are needed.Demand for the low energy consumption, small area for the electronic chipsets and high speed analog-digital convertor, caused the using of dynamic comparator rising, achieving the high speed and low energy consumption.

In this article the lag time of comparators has been assessed, using the analytical analysis.The designers and engineers can determine the effective parameters on lag time and other parameters in comparator performance, using the analytic analysis. A novel comparator in addition to analytic analysis has been designed with an innovative architecture and its performance has been compared with Strong Arm and Double Tail comparators. The comparators are circuits that can recognize the magnitude or the exiguity of signals from the zero reference, maximum or minimum amounts (Tony Chan Carusone , et .al ,2012).Meanwhile, increasing the sensitive and portable sensors in strategic professions such as medicine, biochemistry and etcetera show the necessity of low voltage, rapid and small comparator existence (Yongfu Li,et .al,2014 and Teknol. Mara,et.al ,2011).

Strong Arm Dynamic comparator

Strong Arm latch has been designed by koubashi in 1993 (Razavi, B. et.al, 2015). This latch is used mainly in analog to digital convertors, amplifiers sense, comparators and the latches with high sensitivity (Nirschl, T. ; Schmitt-Landsiedel, D., 2004). These comparators are considerable because of their high input impedance, symmetric swinging output, no static power consumption and the input offset voltage origination from the pair transistors differential input (Razavi, B.et.al, 2015). The circuit performance is as below:

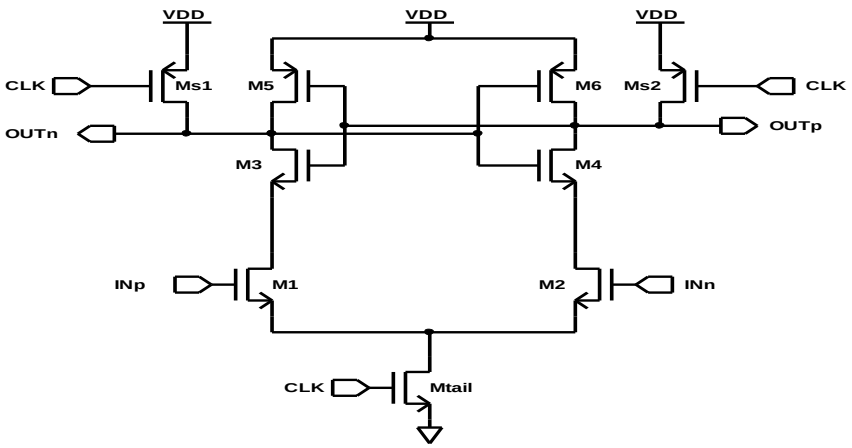


Fig1. Strong Arm comparator Schematic

At reset state, when the CLK=0V, the Mtail transistor turned off and Ms1 and Ms2 transistors turned on then. This causes that the OUTp and OUTn nodes being charged for VDD amount. In comparing state when CLK= VDD, the Ms1 and Ms2 transistors turned off and Mtail turned on. At this moment the voltage of OUTp and OUTn nodes is stail equals to VDD that compared based on INp and INn voltage deference. For example if the INp> INn, then the current will be Ip>In, that causes the rapid OUTn node discharged towards the OUTp node. When the OUTn node voltage reaches to VDD-Vthp amount, the OUTp node has not been discharged that makes the M4 transistor off and the M6 transistor ON. This charges the OUTp node for VDD amount. Finally the M5 transistor turned off and M3 turned on, charging the OUTp node for VDD amount, using the latch positive feedback property. This causes the f OUTn node ull discharge to zero; The vice versa situation will be occurred when the INp< INn.

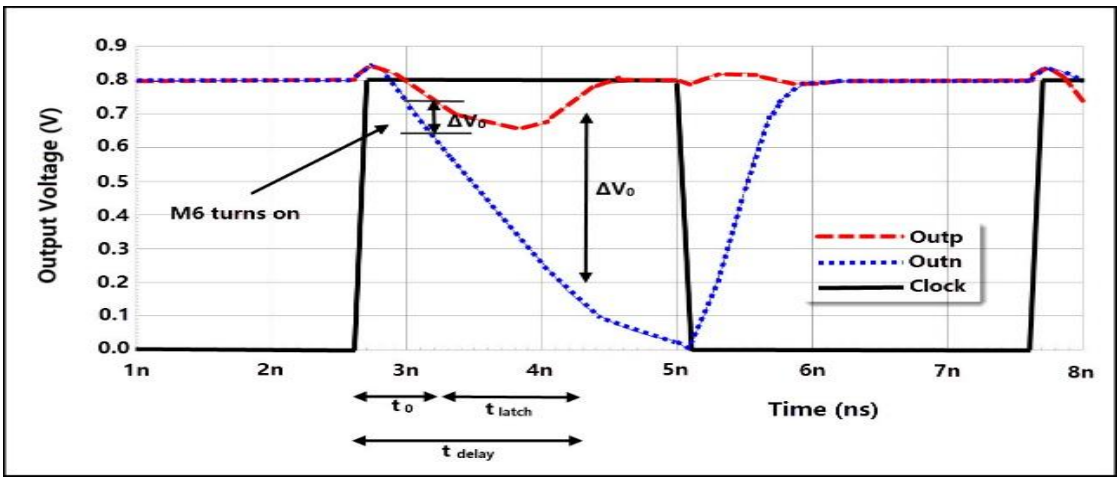


Fig2. The Strong Arm comparator transient response

As it can be seen in figure 2, the lag time consists of two part, t_0 and t_{latch}

$t_{delay} = t_0 + t_{latch}$ (1)

t_0 shows the CL Capacitor discharge connected toOUT_p and OUT_n nodes. Until the first transistor of Chanel P (M5/M6) turned on, when the INp >INn, the I_p current will be greater than I_n,causes the rapid discharge of OUT_n node than the OUT_p. the lag time is stated as below:

$$t_o=\frac{CL|Vthp|}{Ip} \cong 2\ \frac{CL|Vthp|}{Itail} \quad (2)$$

In relation 2 for the small changes, ΔI_{in}, it can be written:

$I_p = I_{tail}/2 + \Delta I_{in} \cong I_{tail}/2$

Second lag time, t_{latch}, relates to the back to back inverters; this time depends on $\Delta V_{out}$and ΔV_0. ΔV_{out} shows the train to train output oscillation at the output discharge (Out_n and Out_p). ΔV_0 shows the internal voltage of the back to back inverters. The lag time of t_{latch}stated as below (Choi, R.Y.-K et.al, 2012.):

$$t_{latch}=\frac{C_L}{g_{m,eff}}\ \ln\left(2\frac{\Delta V_{Out}}{\Delta V_0}\right) \quad (3)$$

As it can be seen the $t_{latch}$is dependent to the ΔV_{out} and ΔV_0 via a Logarithmic relationship. And $g_{m.eff}$ is the effective conductivity of two back to back inverters.ΔV_0 is the voltage difference ofOut_n and Out_p at $t=t_0$ and obtained as below:

$$\Delta V_0=\left|Out_p\ (t=t_0)-Out_n\ (t=t_0)\right|$$
$$=V_{thp}-\frac{I_n t_0}{C_L}$$
$$=V_{thp}\left(1-\frac{I_n}{I_p}\right) \quad (4)$$

In relation 4 the current difference, $\Delta I_{in} = \left|I_p - I_n\right|$, is so smaller than I_p and I_n, therefore it is possible to approximate the I_p with the half of I_{tail}, then we have:

$$\Delta V_0=\left|V_{thp}\right|\frac{\Delta I_{in}}{I_p} \approx 2\left|V_{thp}\right|\frac{\Delta I_{in}}{I_{tail}} \quad (5)$$
$$= 2\left|V_{thp}\right|\frac{\sqrt{2\beta_{1,2}I_{tail}}}{I_{tail}}\Delta V_{in}$$

$=2|V_{thp}|\sqrt{2\frac{\beta_{1,2}}{I_{tail}}}\,\Delta V_{in}$ (6)

$\boldsymbol{\beta}_{1,2}$ is the conductivity coefficient of M1 and M2 transistors. Substituting the 3 and 6 relations we have:

$t_{latch}=\frac{C_L}{g_{m,eff}}\ln\left(\frac{\Delta V_{Out}\sqrt{I_{tail}}}{\Delta V_{in}\sqrt{2\beta_{1,2}}|V_{thp}|}\right)$ (7)

The output voltage oscillation, $\Delta V_{0ut} = VDD/2$ gained from the internal voltage difference ΔV_0 at the output voltage drop (Out_p and Out_n). Therefore the half of voltage resource considered the threshold inverter or SR latch (Babayan-Mashhadi, 2013). Substituting the relations 1, 2 and 7 we have:

$t_{delay}= 2\frac{C_L|V_{thp}|}{I_{tail}}+\frac{C_L}{g_{m,eff}}\ln\left(\frac{VDD\sqrt{I_{tail}}}{2\,\Delta V_{in}\sqrt{2\beta_{1,2}}|V_{thp}|}\right)$ (8)

As it can be seen in relation 8, the lag time dependence on some factors. The lag time has a direct relation to the load capacitor (C_L). The effect of I_{tail} is obvious in t_0 and t_{latch} it has an inverse relation to t_0 and a direct relation to t_{latch} and$I_{tail}^{\frac{1}{2}}$. Generally the lag time is reduced with increasing in I_{tail}. Also the effect of ΔV_{in} and ΔV_{out} is obvious in t_{latch}.V_{in} voltage has an indirect relation to the lag time, when the Vin increases the I_{tail} will increase and the internal voltage decreases subsequently. Unit current tail of this comparator is the negative property. Tail current decreasing causes the I_p and I_n reduction subsequently ($I_{tail} = I_p + I_n$) and it rises the lag time. For the lag time reduction it is better to increase the I_{tail} (D. Shinkelet. al, 2007).

Double tail dynamic comparator

In this comparator the less back to back transistors have been used than the Strong Arm comparators. Therefore this comparator can have a good performance in low voltage.

This comparator consists of two current tail that upper tail is independent of Vcm (shared voltage). Also it uses two o'clock for the activeness and inactiveness of initial and middle Amplifier that are used as the latch input for the kickback noise effects reduction (Figueiredo, P.M,2006 and Shinkelet. al , 2007).

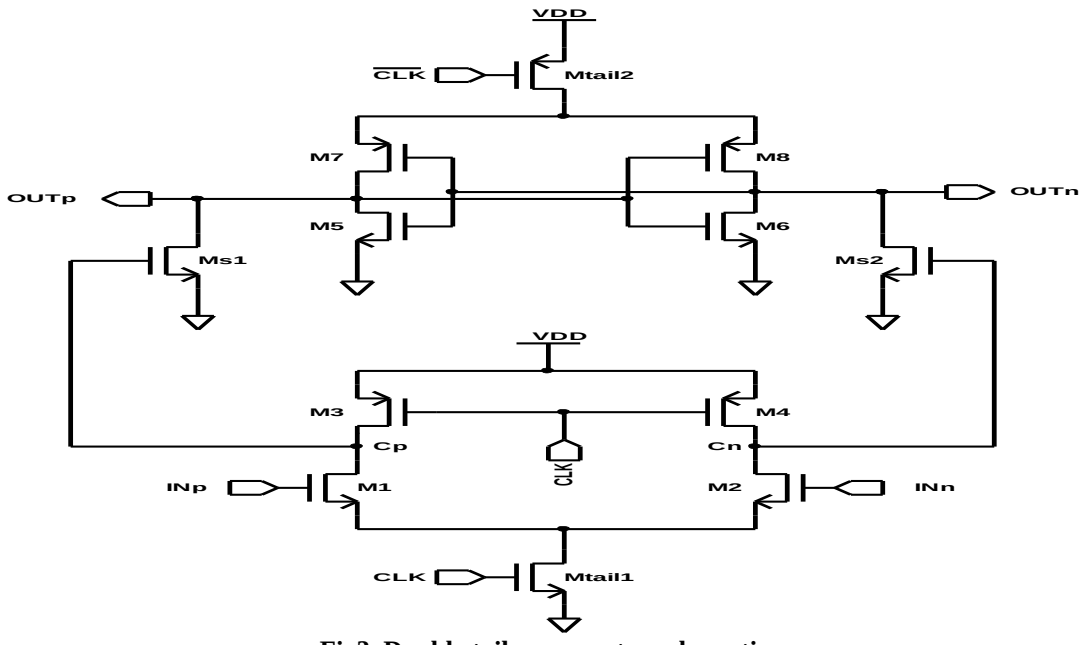


Fig3. Double tail comparator schematic

Circuit performance is as below. The beginning state of circuit is in CLK=0, in this situation the M_{tail1} and M_{tail2} turned off and M_3 and M_4 turned on. The C_p and C_n nodes being charged via the M_3 and M_4 transistors equal to VDD.As a result of this, the middle class, as a key that consists of M_{S1} and M_{S2} transistors, turned on and caused the $Out_p$and Out_ndischarging to the zero.The comparing situation take place when the CLK=VDD.In this situation the M_3 and M_4 transistors turned off while the M_{tail1} and M_{tail2} turned on. In setting time, the voltage of C_n and C_p nodes equal to VDD. The C_n andC_p nodesdischarge to the zero with $\frac{I_{tail\,1}}{C_{C_{n,p}}}$ velocity based on input voltage difference (IN_p and IN_n).

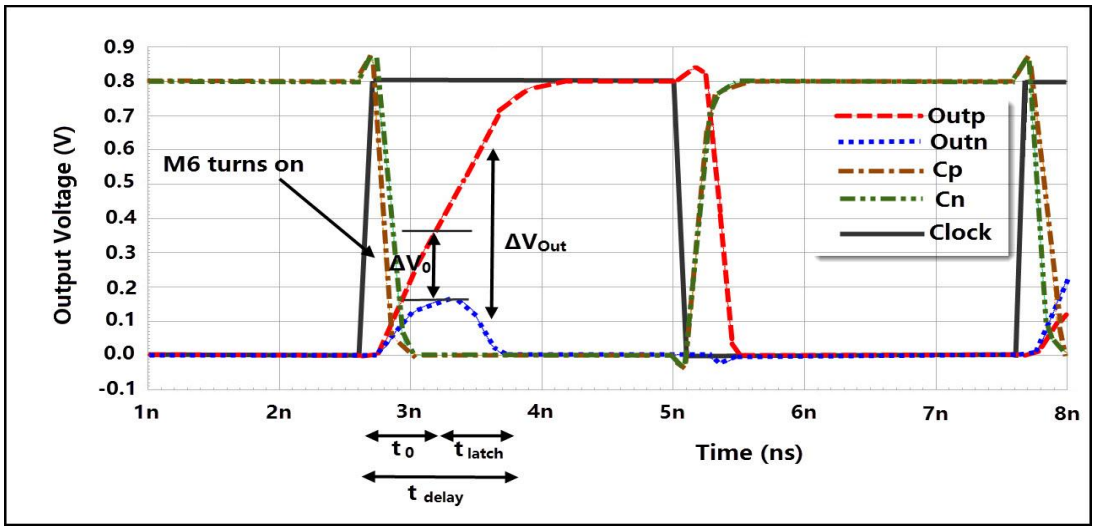


Fig4. Transient response of double tail comparator

In this comparator the lag time based on relation 2 consists of two part. First part relates to the capacitor discharging ($C_{L_{1,2}}$), connected to $Out_{p,n}$ until the first voltage of n-channel transistor reaches to the V_{thn} to turn on (t_0).Therefore the t_0 obtained as below:

(9)$2\frac{V_{thn}C_{L\,out}}{I_{tail\,2}} = t_0 = \frac{V_{thn}C_{L\,out}}{I_{D1}}$

I_{D1} current in this transistor considered as M_6. When the first n-channel transistor turned on, the Out_nnode voltage discharged to the zero, then the M_5 transistor turned off and M_7 turned on, caused the Out_p node charging to the VDD amount. The lag time of latch obtained from relation 3. Calculating the internal voltage difference of ΔV0 at t0 is as below:

$\Delta V_{0=}\left|Out_p\ (t=t_0) - Out_n\ (t=t_0)\right|$

$= V_{thn} - \frac{I_{D2}t_0}{C_{L\,out}}$

$= V_{thn}\left(1-\frac{I_{D2}}{I_{D1}}\right)$ (10)

In upper relation the current difference, $\Delta I_{in} = |I_{D1} - I_{D2}|$, is so lesser than I_{D1} and I_{D2}.Therefore the I_{D1} can be approximated by the half of I_{tail2} current. Then it can be written:

$\mathbf{\Delta I_{latch}} = |I_{D1} - I_{D2}| = g_{mS\,1,2}\Delta V_{cp/cn}$ **(11)**

Having the relation 10 and 11:

$\Delta V_0 = V_{thn}\frac{\Delta I_{latch}}{I_{D1}} \approx 2V_{thn}\frac{\Delta I_{latch}}{I_{tail\,2}}$

$= 2V_{thn}\frac{g_{ms\,1,2}}{I_{tail\,2}}\Delta V_{cp/cn}$ (12)

As it can be seen in relation 12, the internal voltage difference (Δ_{V0}) at the moment t_0 is dependent on conductivity coefficient of M_{s1} and M_{s2} transistors and the output voltage difference of first class.The output voltage difference of first class obtained as below:

$\Delta V_{cp/cn} = \left|V_{cp}\ (t=t_0) - V_{cn}\ (t=t_0)\right|$

$= t_0\frac{|I_p - I_n|}{C_{L\,cp,n}}$

$= t_0\frac{g_{m\,1,2}\Delta V_{in}}{C_{L\,cp,n}}$ (13)

In these relations the I_p and I_n relates to the M1 and M2 transistor currents that discharge the C_p and C_n nodes.

$\Delta I_{in} = g_{m1,2}\Delta V_{in}$ (14)

From the relations 12, 13 and 14 we have:

$\left(2\frac{V_{thn}}{I_{tail\,2}}\right)^2\Delta V_0 = \frac{C_{L\,Out}}{C_{Lcp,n}}\ g_{ms\,1,2}g_{m\,1,2}\Delta V_{in}$ (15)

The internal voltage difference of latch at t0 moment, depends on input conductivity coefficient of middle class and the capacitor ratio of$C_{L\,Out}$, $C_{Lcp,n}$ and$I_{tail\,2}$. The output voltage oscillation, ΔV_{out}=VDD/2, obtained from the internal voltage, ΔV_0, at the output voltage drop. Therefore the half of voltage resource considered as the threshold inverter or the SR latch (Babayan-Mashhadi, 2013). The lag time obtained from the relations 1, 9 and 15.

$t_{delay} = t_0 + t_{latch}$

$$= 2\frac{V_{thn}C_{L\,Out}}{I_{tail\,2}} + \frac{C_{l\,Out}}{g_{m,eff}}\mathrm{Ln}\left(\frac{\Delta V_{Out}}{\Delta V_0}\right)$$

$$=2\,\frac{V_{thn}C_{L\,Out}}{I_{tail\,2}} + \frac{C_{L\,Out}}{g_{m,eff}}\,\mathrm{Ln}\left(\frac{V_{DD}.C_{Lcp,n}.{I_{tail\,2}}^2}{C_{L\,Out}.g_{mS\,1.2}g_{m\,1,2}\Delta V_{in}{4V_{thn}}^2}\right) \qquad (16)$$

Designed dynamic comparator

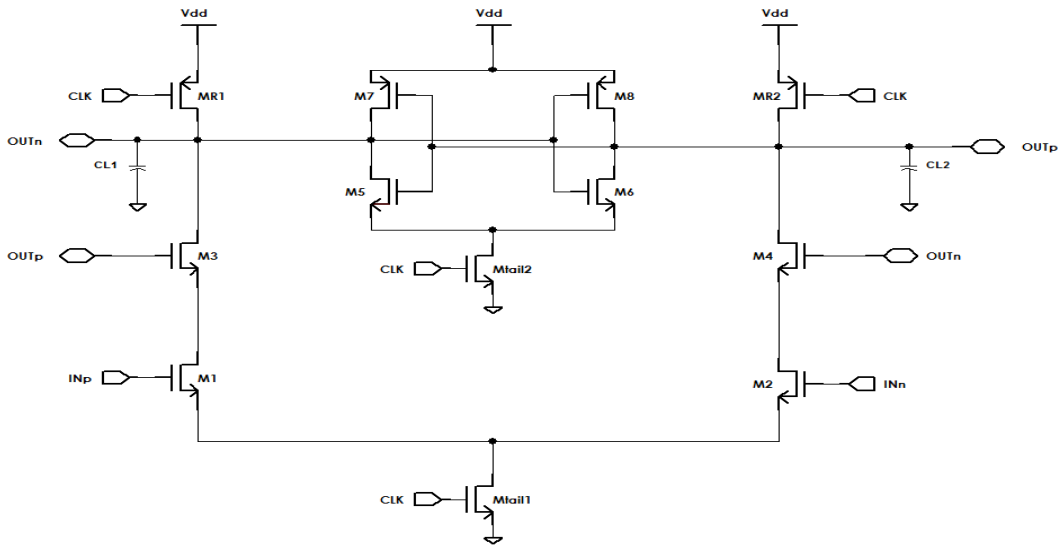
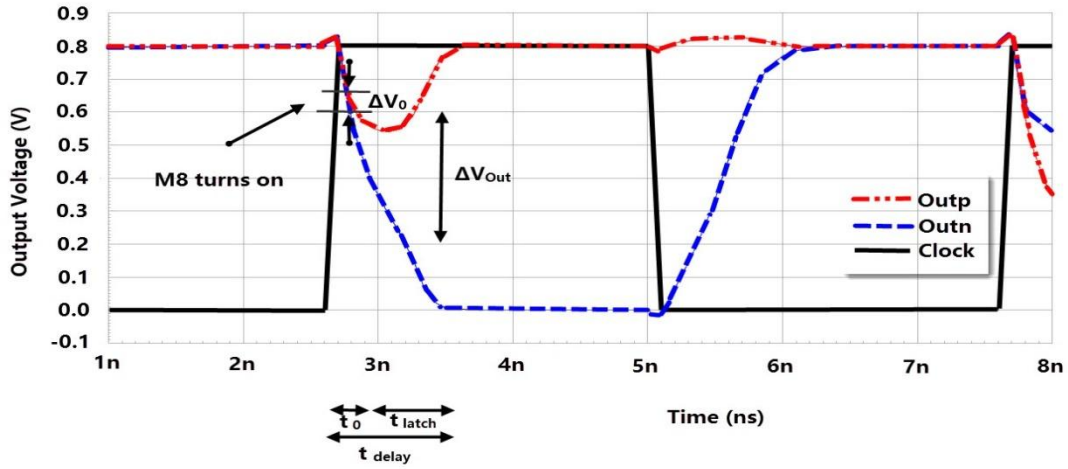


Fig5. The designed comparator schematic

In this comparator the start state is when the CLK=0V, in this condition the M_{tail1} and M_{tail2} transistors turned off while MR1 and MR2 transistors turned on. In this state the Out_p and Out_n outputs are charged to VDD. In set state, when the CLK=VDD, the MR1 and MR2 are off while M_{tail1} and M_{tail2} turned ON. In this situation the I_p current is bigger than I_n, causes the rapid discharge of Out_n node than the Out_p. When the Out_n voltage reaches to the VDD-V_{thp} the comparing is begun that M6 transistor turned off and M8 turned ON. In this state Out_p charged to VDD, causes the M7 transistor turned off and M5 turned ON, causes the feedback stability in latch.This comparator consists of two part same as the previous comparators.



The first part (t_0), relates to the capacitor discharge time. Upon to relation 2:

$$t_o=\frac{CL|Vthp|}{Ip} \cong 2\frac{CL|Vthp|}{(I_{tail\,1}+I_{tail\,2})} \qquad (17)$$

Based on relation 17, the capacitor discharge time has the inverse relation to the total current of two current tail, causes the rapid discharge of capacitor and lag time reduction subsequently. The second part (t_{latch}) relates to the latch lag time. Upon to the relation 3:

$$t_{latch}=\frac{C_L}{g_{m,eff}}\ln\left(2\frac{\Delta V_{Out}}{\Delta V_0}\right)$$

$\Delta V_{0=}\left|\text{Out}_p\ (t=t_0) - Out_n\ (t=t_0)\right|$

$=V_{thp}-\frac{I_n t_0}{C_L}$

$=V_{thp}\left(1-\frac{I_n}{I_p}\right)$

$=V_{thp}\left(\frac{\Delta I_{in}}{I_p}\right)$

In upper relation the current difference, $\Delta Iin = \left|I_p - I_n\right|$, is very smaller than I_p and I_n; therefore the I_p can be approximated by the half of $I_{tail1}+I_{tail2}$ current. Therefore it can be written:

$\square$ $\mathbf{V_0=2.\ V_{thp}\left(\frac{\Delta I_{in}}{(I_{tail\ 1}+I_{tail\ 2})}\right)}$ **(18)**

From the relation 11 and 18:

$\Delta V_0 = 2.V_{thp}\left(\frac{g_{m1,2}\Delta_{in}}{(I_{tail\ 1}+I_{tail\ 2})}\right)$ (19)

From the relation 3 and 19:

$t_{latch} = \frac{C_L}{g_{m,eff}}.\ln\left(\frac{(I_{tail\ 1}+I_{tail\ 2})\Delta V_{Out}}{V_{thp} g_{m1,2}\Delta V_{in}}\right)$ (20)

As it can be seen in relation 20, the latch lag time has a direct relation to the total current of tail 1 and 2, also it has an inverse relation to M1 and M2 transistors.In this relation the tail 1 current is dependent on input voltage while the tail 2 current is a constant current resource that active and inactive by a clock. The output voltage oscillation, ΔV_{out}=VDD/2, obtained from the internal voltage, ΔV_0, difference at the output voltage drop.So, the half of voltage resource considered as the threshold inverter voltage or SR latch (Babayan and Mashhadi, 2013). We have from 1, 17 and 20:

$t_{delay} = t_0 + t_{latch}$

$t_{delay} = \frac{2C_L\left|V_{thp}\right|}{(I_{tail\ 1}+I_{tail\ 2})} + \frac{C_L}{g_{m,eff}}.\ln\left(\frac{VDD\,(I_{tail\ 1}+I_{tail\ 2})}{2V_{thp} g_{m1,2}\Delta V_{in}}\right)$ (21)

As it is obvious in relation 21, the lag time has been reduced than two aforementioned relations, that simulation results approves it.

The comparator's kickback noise

Basically in comparator circuits, the huge voltage changes in latch nodes is coupled via the para static capacitors of transistor to the comparator circuit entrance. This operation causes the input voltage confusion in comparator and the error in its performance. This error in comparators, is called kickback noise (Figueiredo, P.M et.al, 2006 and Babayan-Mashhadi, 2013).The Strong Arm and the designed comparators have the higher kickback noise error, because they are not isolated from the latch comparator, while the double tail comparator has the small kickback noise because it is isolated from the latch comparator.

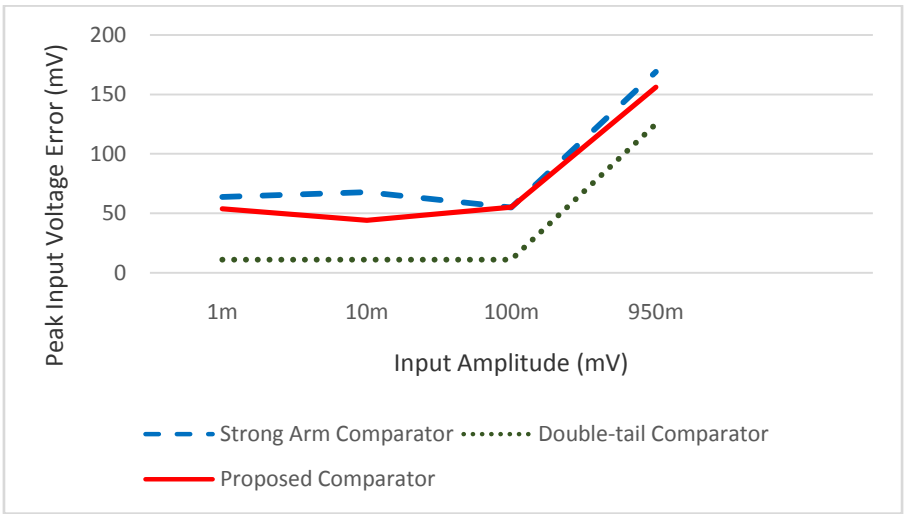


Fig7. The kickback noise range versus the input voltage domain

Offset voltage of comparators

Offset voltage is the difference of input DC voltage consists of a comparator, APMP and amplifier. Offset voltage in low voltage comparator causes the logical level and undesirable behavior in digital circuit output, subsequently it causes the incorrect performance of comparators and the higher energy consumption.

Therefore the offset voltage should be studied and evaluated in very sensitive applications. The comparators have been optimized in this study and the transistor's parameters have been considered that an offset standard deviation is equal to 4(mV) with the shared input voltage equal to 1.1(V) (Babayan-Mashhadi, 2013 and D. Shinkelet. al, 2007).

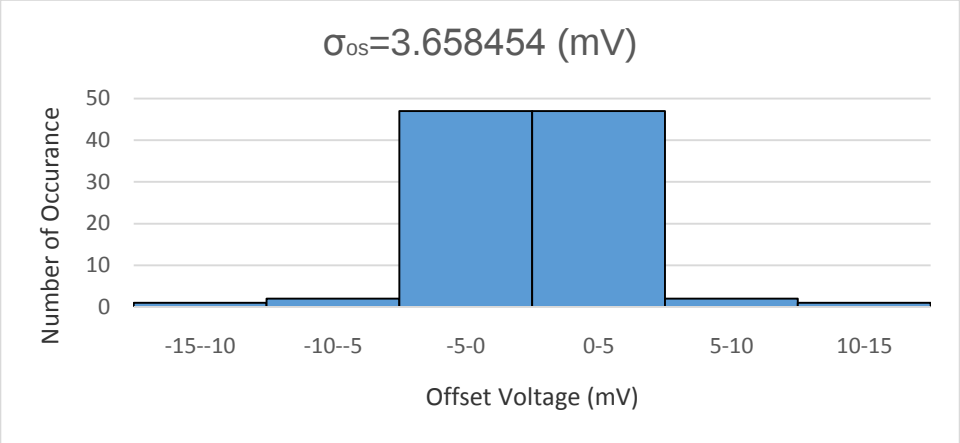


Fig8. The suggested comparator offset (50 times iteration)

Simulation

In this study the simulation has been performed using the CMOS 0.18um technology, comparing the three Strong Arm, Double Tail and suggested comparator. In figure 8 the lag time and in figure 9 the velocity versus the constant voltage resource (VDD) has been plotted. Also in figure 10 the lag time and in figure 11 the velocity upon to the voltage resource (Vcm, Common Mode Voltage) has been plotted.

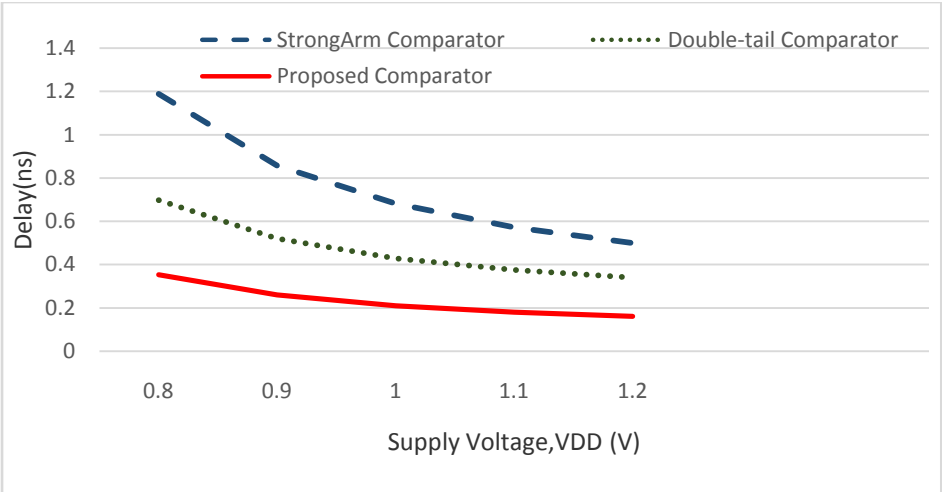


Fig8. Simulation of lag time (V_{cm}=VDD-0.1(V), □ V_{in}=50(mV))

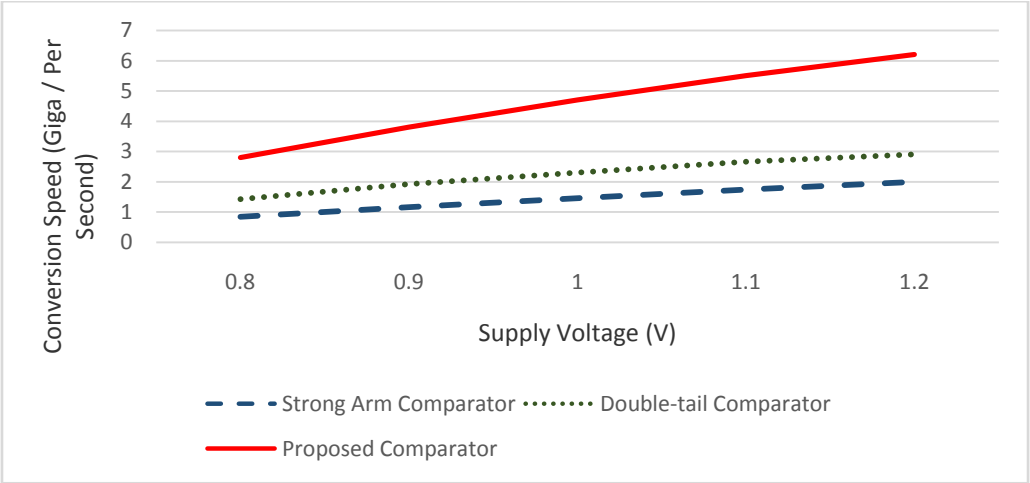


Fig9. Simulation of speed conversion (V_{cm}=VDD-0.1(V), □ V_{in}=50(mV))

Based on figure 8 the lag time decreases with the voltage resource increasing also the lag time of suggested comparator is lesser than two others as the lag time in comparator 1 at VDD=1.2 (V), increases from 161.037(ps) to 1.18659 (ns) at VDD=0.6 (V). Upon to figure 9 the speed of suggested comparator is more than two others as it speed increases at VDD=0.8(V) from 2.8G/s to 6.2G/s at VDD=1.2(V).

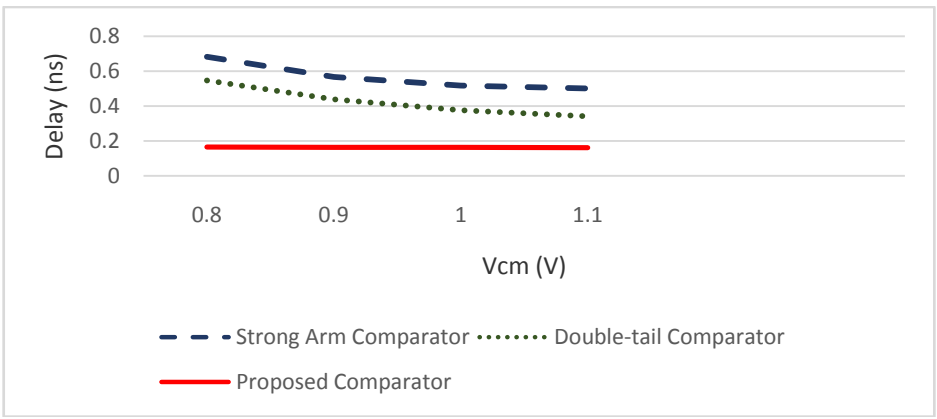


Fig10. Lag time simulation (□ Vin= 50(mV), VDD=1.2(V))

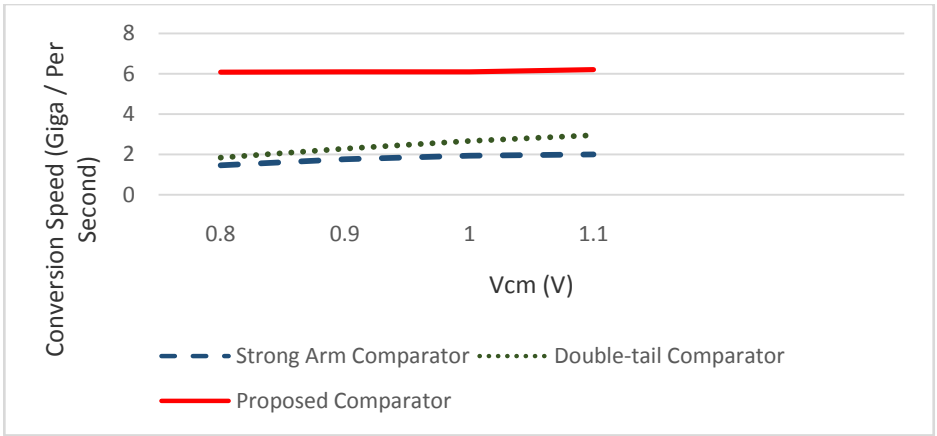


Fig11. Speed conversion simulation (□ Vin= 50(mV), VDD=1.2(V))

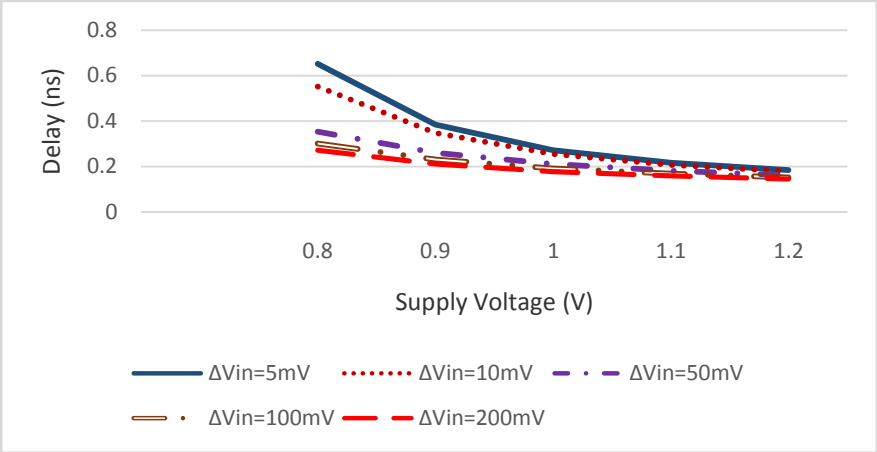


Fig12. Suggested comparator lag time versus the voltage resource

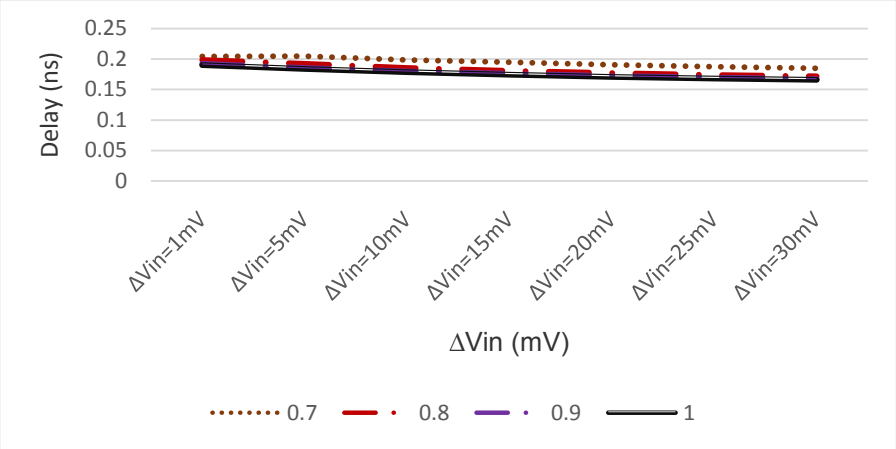


Fig13.Suggested comparator lag time versus the input voltage resource domain

Table1. The suggested comparator properties

amount	parameter
180-nm CMOS	technology
1.2 V	Voltage resource
15.194 (µW)	The amount of energy consumption in 100MHz frequency (Vcm=1.1 V , ΔVin= 25 mV)
240.452 (ps)	The worst state of lag time (Vcm=0.6 V , ΔVin= 1mV)
3.658454 (mV)	(1-sigma) , (σos) The input voltage offset
2.44 (fJ)	energy efficiency (Vcm=1.1 V , ΔVin= 25 mV)
151.94 (fJ)	Energy in each cycle (Vcm=1.1 V , ΔVin= 25 mV)
6.2 (Giga/per second)	(Vcm=1.1 V , ΔVin= 25 mV) Speed
23.45 (um) * 14.505 (um)	Approximated chipset area

Table2. Comparing the comparator properties

Suggested Comparator	Double Tail	Strong Arm	Comparator properties
900MHz	1.8GHHz	900MHz	Sampling maximum frequency
44 (mV)	6(mV)	55(mV)	Kickback noise @(ΔVin=10mV)
151.94 (fJ)	202.81 (fJ)	114.1 (fJ)	Each cycle energy (Vcm=1.1 V) (ΔVin= 25 mV)
2.44 (fJ)	6.74 (fJ)	10.311 (fJ)	Energy efficiency
6.2 (Giga/per Second)	2.94 Giga/per second))	2 (Giga/per second)	speed (Giga/per second)
3.658454 (mV)	4.357 (mV)	4.02 (mV)	Input voltage offset (Vcm=1.1V)(1-sigma) , (σos)
23.45 (um) * 14.505 (um)	31.295 (um) * 13.875 (um)	25.41 (um) * 14.77 (um)	Chipset approximated area

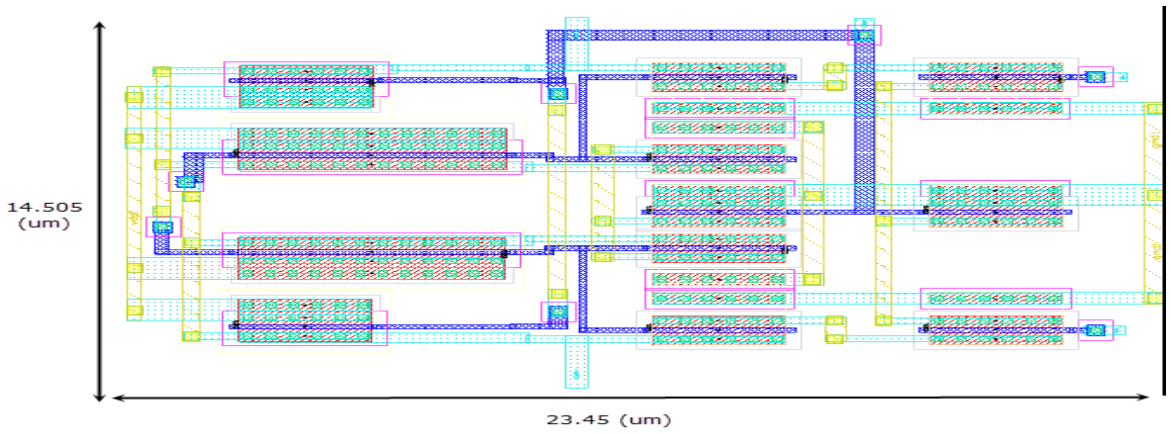


Fig14. The suggested comparator layout

II. Conclusion

In this article, the complete analysis of dynamic comparators has been studied and their terms have been extracted. Also two Strong Arm and Double Tail comparators have been analyzed, and based on analytical analysis a fast and optimized low voltage comparator has been introduced. The simulation results and the comparing performance table show the better performance of suggested comparators than the Strong Arm and Double Tail comparators.

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